Design of a Near Threshold Low Power DLL for Multiphase Clock Generation and Frequency Multiplication

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***Abstract*- In this paper we present an ultra low power all digital DLL operating near threshold voltage with lock in range of 80 - 200MHz. The DLL is immune to false locking problem and dithering around the lock point. Besides clock de-skewing and multiphase clock generation it can multiply the frequency by four. The DLL is implemented in 45nm PTM and operates at 0.7 V and dissipates 120uW at 200MHz**.

Keywords- all digital DLL, de-skewing, frequency multiplication.

I. INTRODUCTION

Delay Locked Loops have become an important component of integrated circuit chips. The main applications of DLL are in multiphase clock generation in system on chip, on chip clock de-skewing and frequency multiplication. Multi-phase clocks are used to process data streams at a bit rate higher than internal clock frequencies in high-speed serial link applications [1]. In microprocessors, multiphase clocks can ease the clock constraints in pre-charged logic to achieve higher operating speed [2]. DLLs are essential in circumventing clock skewing problem in a chip, which is unavoidable due to finite propagation delay, loading effect and variation due to process, voltage and temperature [3]. An edge combiner can combine the multiple clock phases and act as a programmable frequency multiplier useful in Dynamic Voltage and Frequency Scaling (DVFS) [4]. DLL`s counterpart, PLLs, are attractive for use as clock multipliers because they provide a simple means of frequency multiplication and can support a programmable multiplication rate. Unfortunately, given an identical noise environment and circuit components, a PLL has higher jitter than a DLL due to phase noise accumulation. Besides no jitter accumulation, a DLL is mostly a single-pole system, does not rely on a high loop bandwidth to correct for jitter and exhibits negligible jitter peaking [5]. Not many papers have treated the argument of an ultra low power DLL before. Liang et al. [6] propose an all digital fast locking programmable DLL based clock generator with short locking time. The input frequency range is 4 to 200 MHz and dissipates 17mW at 3.3 V. Considering the frequency range the power dissipation is quite high. Mesgarzadeh et al. [7] describe an all digital DLL operating in the open loop mode. The system operates in open loop mode during normal operation, but if there is a phase mismatch, it shifts to closed loop architecture and remains in the closed loop form until the phase mismatch is eliminated. This work was designed in 90nm technology with a 1V voltage supply, operates at 2 GHz and has an average power consumption of 7mW. Although this is one of the most efficient reported DLL architectures, further power reduction is possible by redesigning the delay cell, phase detector and counter control logic, which we address in this paper.

The contribution of this paper are 1) The designed DLL operates at near threshold voltage of 0.7 V within 83 - 200MHz. 2) The phase detector generates control signals at the critical clock edges which control the counter. 3) The counter is equipped with power and clock gating which reduces power. During standby mode the state of the counter is held in a latch. If due to PVT variation the DLL locks out of synchronism, the counter gets powered again and starts from the latched value. 4) An Xor gate based edge combiner multiplies the frequency by four. In section II the DLL architecture is explained. In section III simulation results are explained.

II. DLL ARCHITECTURE

The DLL consists of a 8 stage delay line, Phase detector, counter and an edge combiner. Figure 1 shows the block diagram. The design of these major components is discussed below.

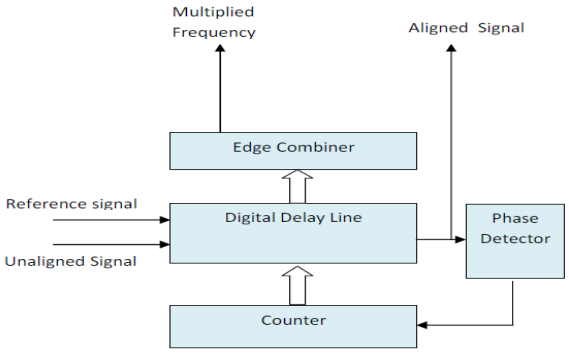

Figure 1: Proposed DLL Block Diagram

A. Phase Detector

The phase detector detects the amount of lead/lag between reference and the clock to be de-skewed. Based on the relative phase difference it generates two control signals – STABLE and UP_DOWN. The STABLE signal causes the counter to hold its current value whereas the UP_DOWN signal controls the direction of counting. The STABLE signal also dictates power control unit which activates power and clock gating to the counter. The phase detector is made of a C2MOS DFF with reset option. In [8] a pre-charge type phase detector is used. But it fails when the phase error exceeds $T_{ref}/2$. The PD used in [7] is critical to the sizing of inverter and keepers which renders it unattractive considering PVT variation. None of these PDs generate a control signal that indicates lock position. Figure 2 shows the block diagram of our designed PD. It effectively samples the leading and lagging phase errors at the falling edge of the reference clock to generate STABLE and UP_DOWN pulses that control the counter. Sampling at the falling edge stabilizes these two signals before the rising edge of the next clock, when the counter updates its state. These two signals are further buffered to be able to drive the counter.

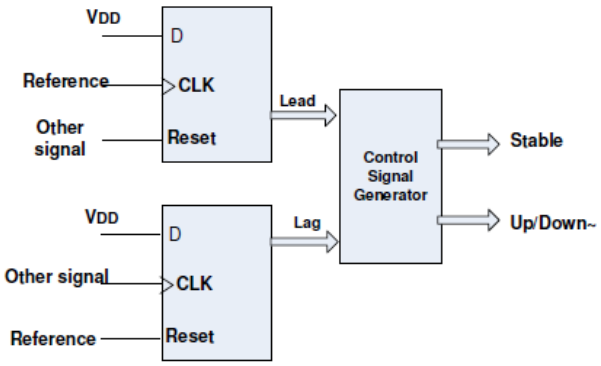

Figure 2: Proposed PD architecture

B. Delay Cell

The inverter in the delay line is sized such that it has a switching threshold exactly at VDD/2. Also, the PMOS and NMOS device in the pull up and pull down path has to be sufficiently wide to charge and discharge the maximum delay line capacitor at the operating frequency. Reduction in the supply voltage increases the delay which impacts the maximum operating frequency. To sustain the operating frequency at reduced voltage, the critical path transistor widths need to be augmented. From simulations at 0.7V and 200MHz PMOS and NMOS width of 295nm and 195nm are required, respectively. This corresponds to an average pull up and pull down resistance of 4.6KΩ. For 200-83 MHz range the time period is between 5ns and 12ns. Per stage total capacitor has to be chosen such that the 8 stage delay aggregates to 12ns or higher (1.5ns or higher single stage).

$$t_d = 0.693 R_{ON} C_L \qquad (1)$$

With $R_{ON} = 4.6\ K\Omega$ total per stage capacitor is 470fF. And this is distributed per cell in binary weighted fashion such that when all the switches are on the total capacitor equals or exceeds this value. With 8 bit control word this corresponds to per bit resolution of 1.84 fF or higher. We choose 2fF as the minimum. These capacitors are implemented as the gate capacitance of mosfet with its source and drain shorted.

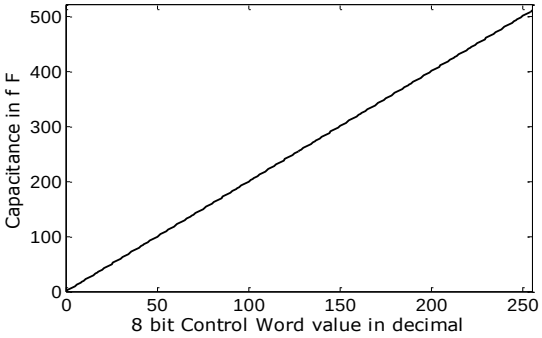

Figure 3: Capacitance vs. Control Word

Table 1: NMOS size for the required capacitors

L	W	Cap effective	Cap ideal
105n	100u	128.7fF	128fF
50n	68u	63.9fF	64fF
50n	31.6u	32fF	32fF
50n	15.1u	15.9fF	16fF
50n	7.5u	8.03fF	8fF
50n	3.75u	4.04fF	4fF
50n	1.855u	1.99fF	2fF

C. Counter

We have designed a synchronous binary up/down counter with asynchronous reset option. The reset signal can load any pre determined value and the counting starts from there. The counter operates perfectly within the desired frequency range of 83-200 MHz whenever the counting direction changes synchronously from up to down (or vice versa) there is an initial one cycle latency at the output. For our maximum operating frequency of 200 MHz this is not an issue. Counters described in [9] can overcome this initial latency at the cost of complex circuit and extra power dissipation. Our counter is equipped with power and clock gating. Whenever the phase error vanishes and the "STABLE" signal from the phase detector goes high, the counter stores its value in a balloon latch. The clock and power supply to the counter is cut with gating transistors. If due to PVT variation clock locks out of synchronism, the counter gets powered up again, starts counting up or down from that stored value. The counter is set to start in the middle of the code word of 0111111. This will provide an initial capacitor of 254fF and equivalent delay of 0.81ns per stage and a total of 6.47ns. Depending on the input frequency and initial clock skew the counter will count upward or downward to reach the codeword that will provide the appropriate delay to ensure lock in. The harmonic lock problem mentioned in [10] has to be considered here. In [10] this problem is solved with complex anti harmonic lock block which absorbs sufficient amount of power. We propose to eliminate the extra circuitry by wisely choosing the initial code word and sampling the phase lead signal at the falling edge to select the direction of counting.

D. Edge Combiner

An edge combiner circuit combines the multiphase clocks, each T/8 apart, and generates a signal having a frequency four times the reference.

III. SIMULATION RESULTS

The DLL is designed in 45nm PTM and simulated in Cadence. The lock in time, control word and corresponding capacitors are reported in table 2 with initial skew of 0.7ns. The DLL simulated at different process corners at 200MHz. The results are summarized in table 3. Table 4 gives a comparison between our design and some of the reported low power digital DLLs. Figure 4 shows the detail waveform.

Table 2: Control word and lock in time at different frequencies

Frequency	Control Word	Capacitor per stage (fF)	Lock in time (ns)
200MHz	01011010	168	223
166MHz	01101010	208	125
142MHz	10011101	248	35
125MHz	10100010	232	120
100MHz	10111000	368	570
83MHz	11101011	470	1300

Table 3: Performance of the DLL at different process corners

Process Corner	Static Phase error (ps)	Lock in cycles at 200 MHz
TT	50	50
SS	55	55
FS	47	50
SF	45	50 (also duty cycle mismatch)
FF	45	60 cycles

Table 4: Comparison of our design with others

	This work	*IEEE Tran 08 [6]*	*JSSC 09 [7]*	*VLSI Symp 07*
Type	All Digital	Digital	Digital	Digital
Process	45nm	0.35 um	90nm	0.13um
Supply	0.7V	3.3V	1V	1.2V
Frequency Range	66 MHZ - 200MHz	4 -200 MHz	2GHz	1.6GHz
Static Phase Error	55ps	N/A	N/A	N/A
Lock in time	Between 28 to 110 Cycles	16 cycles	N/A	N/A
Power	120uW	17mW	7mW	6mW

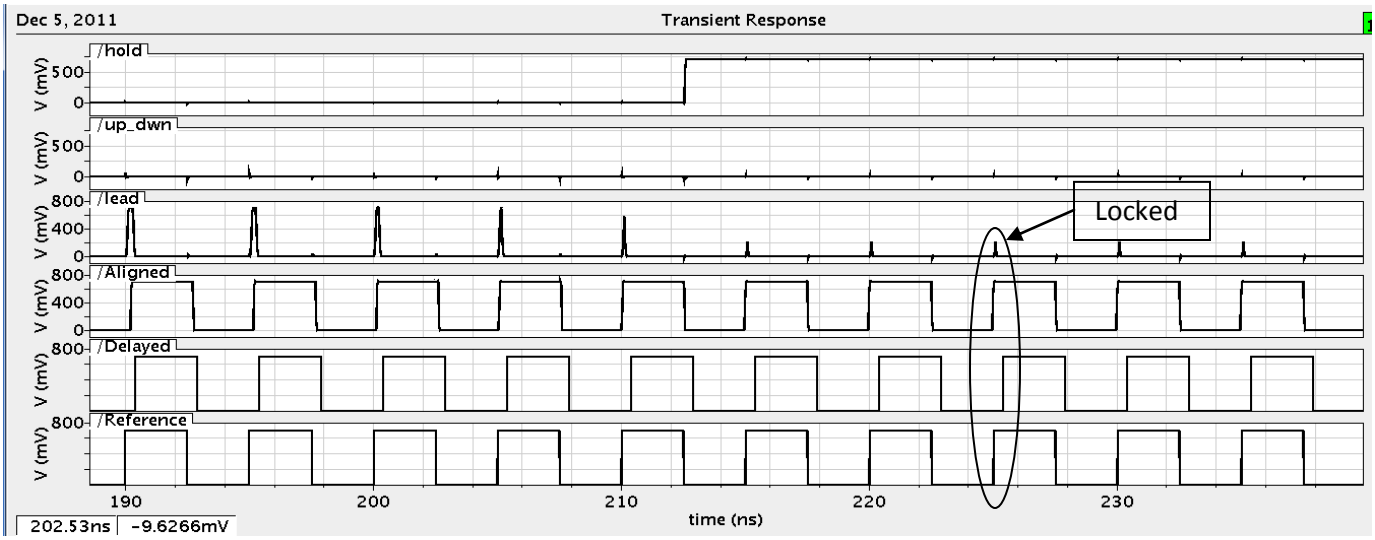

Figure 4: Complete Waveform

IV. CONCLUSIONS

We have designed an ultra low power DLL operating in 83MHz-200MHz at 120uW. The designed DLL functions across all the process corners.

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